Research Article

An Embedded FPGA Design for Double-Time-Over-Threshold (DToT) Measurement

Aydin Tarik Zengin

***Abstract*—This study presents a novel embedded FPGA design utilizing Time-over-Threshold (ToT) and Double-Time-over-Threshold (DToT) methods, addressing the limitations of traditional analog-to-digital converters (ADCs). The ToT method has gained popularity due to its advantages in power consumption, cost, and integration, yet it faces challenges such as energy vs. time resolution trade-offs and signal nonlinearity. The proposed DToT method aims to mitigate these issues by employing two thresholds, offering improved energy resolution and reduced nonlinearity compared to single-threshold ToT methods.**

The system is implemented on a Zynq System-on-Chip (SoC) that integrates an FPGA with an ARM CPU, enabling dynamically adjustable thresholds, high-precision timing measurements, and flexible data processing capabilities. The evaluation was conducted using a CAEN DT4800 Digital Detector Emulator, which generated signals from a 3-inch NaI detector exposed to a ^{22}Na radioactive source. The results demonstrate the superior precision of the DToT method, particularly at lower energies, with σ/μ ratios of 1.82% and 3.82% for the 511 keV and 1275 keV peaks, respectively.

This FPGA-based approach provides a versatile and high-precision solution for instrumentation applications, offering significant advantages over traditional ADCs and single-threshold ToT methods. The integration of an ARM CPU with FPGA logic allows for flexible and tunable signal processing, making it suitable for a wide range of applications, including particle physics experiments, medical imaging systems, and industrial sensors. The study underscores the potential of DToT for high-resolution spectroscopy and suggests areas for future research, such as optimizing the system for specific experimental setups in scintillation gamma cameras or positron emission tomography (PET).

Index Terms— **Time-over-threshold (ToT) measurement, Double time-over-threshold (DToT) measurement, Digital signal processing, Field programmable gate arrays (FPGA), Nuclear spectroscopy.**

I. Introduction

TIME-OVER-THRESHOLD (ToT) has become a popular alternative to traditional analog-to-digital converters (ADCs) for signal processing in particle detectors. It has many advantages regarding power consumption, cost, and integration. Converting input charge into a digital pulse with a corresponding time width without needing an independent ADC has benefits in terms of circuit integration and power consumption [1–3].

Recent advancements in time-over-threshold (ToT) and double-time-over-threshold (DToT) methods have shown promise in improving energy resolution and reducing signal nonlinearity in nuclear spectroscopy applications. A recent study demonstrates the effectiveness of a 64-channel ASIC design for the PANDA experiment, highlighting the potential of ToT-based techniques in high-energy physics [4].

In comparison to traditional ADCs, ToT methods offer significant advantages in terms of power consumption, cost, and integration. However, single-threshold ToT methods suffer from limitations such as energy vs. time resolution trade-offs and signal nonlinearity [2,12,13]. These limitations can degrade the detector's energy resolution, especially at high count rates [14]. Multi-threshold ToT (MToT) methods have been proposed to address these issues [2,15–19], but they often require complex calibration procedures and may still exhibit nonlinearity [17–20]. The double-threshold ToT (DToT) method, as implemented in this work, provides a balance between simplicity and performance, offering improved energy resolution and reduced nonlinearity compared to single-threshold methods [5,15,16]. Additionally, DToT avoids the complexity of MToT methods, making it a more practical solution for many applications.

This paper presents an embedded Field-Programmable Gate Array (FPGA) design for Time over Threshold (ToT) measurement, implementing both the traditional single ToT and the widely used double ToT (DToT) methods. Our approach aims to benefit from ToT while mitigating its limitations, a power-efficient and cost-effective solution to extract signal amplitude from particle detectors. The proposed FPGA design can estimate the pulse height using only two ToTs, potentially simplifying the readout process while maintaining accuracy. By implementing this design in an FPGA, I provide a flexible and tunable platform that can be adapted to many particle detection applications [16]. I used a signal emulator to estimate the pulse height spectrum from a 3-inch NaI detector read out with a photo-multiplier tube with a ^{22}Na radioactive source [21].

II. Methods

A. Pulse Height Estimation by Using ToT

The principle of Time over Threshold (ToT) measurement is illustrated in Fig. 1. The graph shows the signal amplitude vs

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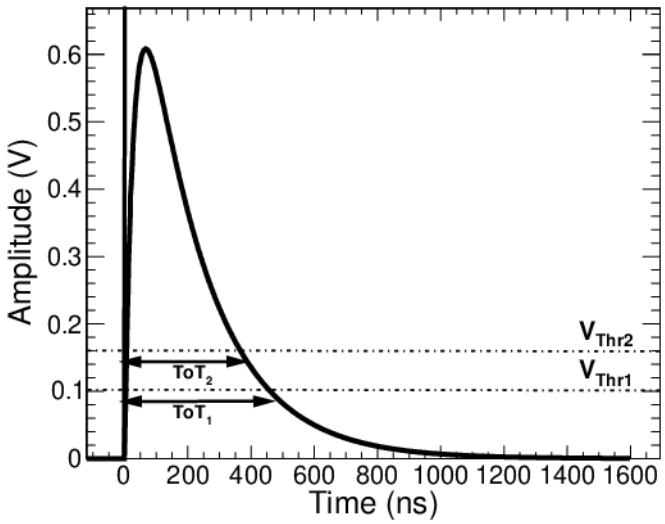


Fig. 1. Double-threshold time-over-threshold signal for a typical detector signal. A lower threshold (VThr1) is set to minimize noise on the detector signal

time with two threshold voltages, VThr1 and VThr2, marked on the y-axis with dashed lines. The ToT intervals ToT1 and ToT2 are times the signal amplitude is above these thresholds. This double threshold is the basis of the DToT measurement used for amplitude extraction from particle detectors.

The pulses from a detector system were emulated using the CAEN DT4800 Digital Detector Emulator. As a pulser, this device can take a known spectrum and generate randomized exponential signals based on characteristic rise and decay times for typical scintillation-based particle detectors.

The input spectrum, shown in Fig. 2, was taken from a 3-inch NaI detector read-out with a photo-multiplier tube in the presence of a ^{22}Na radioactive source [21].

The ADC counts in the input spectrum were converted into a voltage range in the detector emulator. Random pulses with 10 ns rise and 8 µs decay times were generated according to the probabilities in the original spectrum, and the output was in Volts.

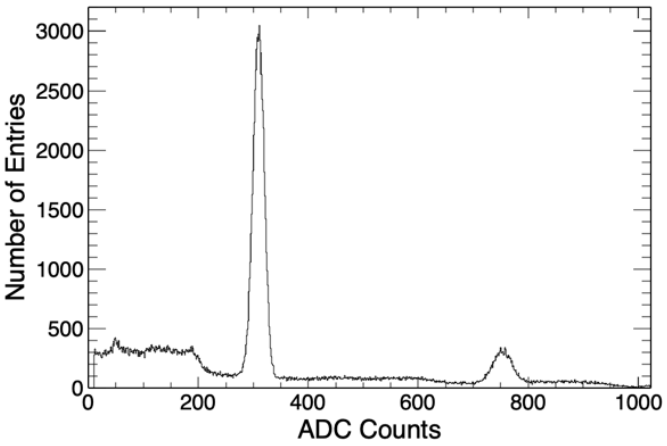


Fig. 2. Input spectrum in ADC counts. Data was obtained from [20].

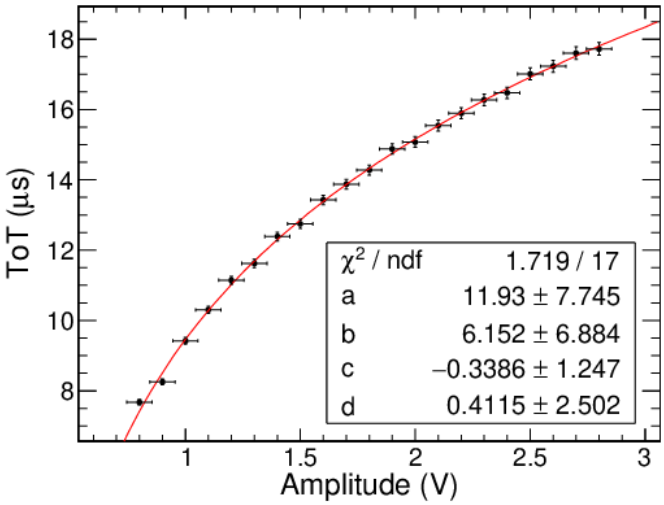


Fig. 3. Input signal amplitude vs. measured ToT. The fit result is indicated with the red line

Fig. 3 shows the input signal amplitude vs $ToT = ToT_1 + ToT_2$ with the fit result in red. The fit function is given in Eq. (1), where x is the input amplitude, a, b, c and d are constants [21]. Parameters a, b, c and d are the signal amplitudes from ToT measurements using the inverse of the fit function. The ToT measurement shows a non-linear relationship with the input signal amplitude, which is crucial for accurately estimating signal amplitude.

$$f(x) = a + b\,ln(x + c) + d[ln(x + c)]^2 \qquad (1)$$

B. DToT Front-End Circuit

DToT was achieved with a circuit composed of two comparators (one for the low and one for the high voltage thresholds) (Analog Devices ADCMP601). The low (VThr1) and high (VThr2) thresholds were provided by the 14-bit DAC (Analog Devices AD9767) controlled by the FPGA. The input signal was split between these comparators. The comparator outputs were connected to FPGA I/Os for digital signal processing.

C. FPGA DToT Implementation

The system's block diagram is shown in Fig. 4. At its core, the system utilizes an FPGA, which implements a DToT measurement technique for high-precision timing analysis of the input signals.

The FPGA is the system's central processing unit, executing the core signal processing algorithms and coordinating overall system functions. It controls the digital-to-analog converters (DACs) for threshold adjustment, implements the pulse-time counting algorithms, and manages the data storage and retrieval. Multiple functions in one FPGA allow for low latency, which is essential for precise timing measurements in nuclear spectroscopy applications.

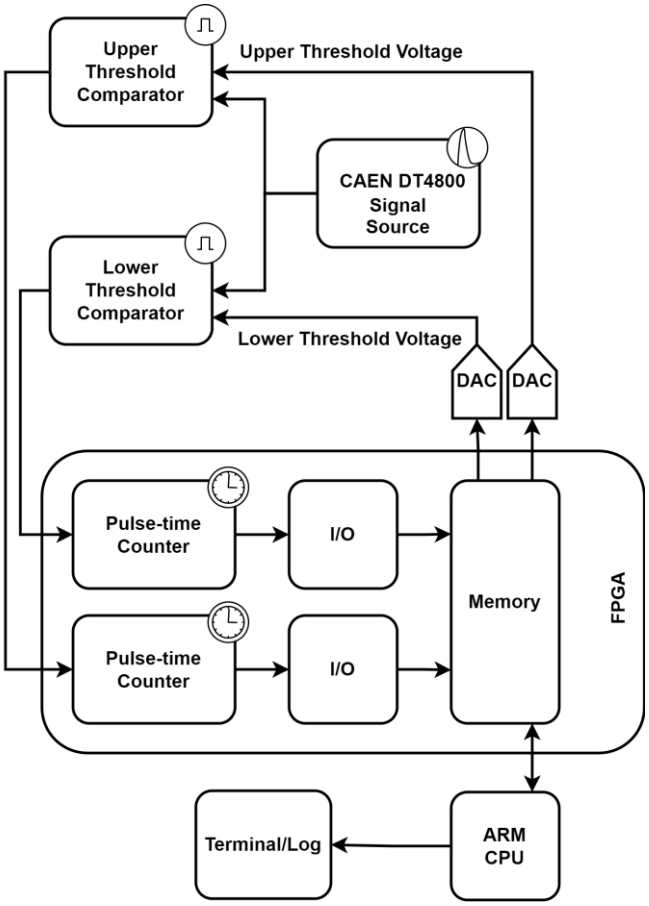


Fig. 4. Block diagram of the FPGA-based DToT measurement system for high-precision nuclear signal processing

The FPGA is paired with an ARM CPU to create a digital signal processing system. The CPU reads data from the FPGA's memory for higher-level data analysis, statistical calculations, and data to be sent to other systems. Having a specialized FPGA and a general-purpose processor allows for post-processing and more system control.

The system architecture combines analog signal conditioning with digital processing to extract timing information from exponential pulses, an essential requirement in nuclear spectroscopy and related fields. The analog front end has adjustable thresholds for optimal signal preparation, and the digital back end, an FPGA and ARM CPU, runs complex data processing algorithms. This hybrid approach allows for precise timing and efficient data analysis to address the specific challenges of nuclear detector signal processing.

The input stage of the system gets an analog signal fed into two separate threshold comparators. These comparators are called the Lower Threshold Comparator and Upper Threshold Comparator and form the basis of the DToT measurement. Each comparator has a dedicated Digital-to-Analog Converter (DAC), so the threshold voltages can be dynamically adjusted. This adaptive thresholding allows the system to accommodate different signal characteristics and experimental requirements.

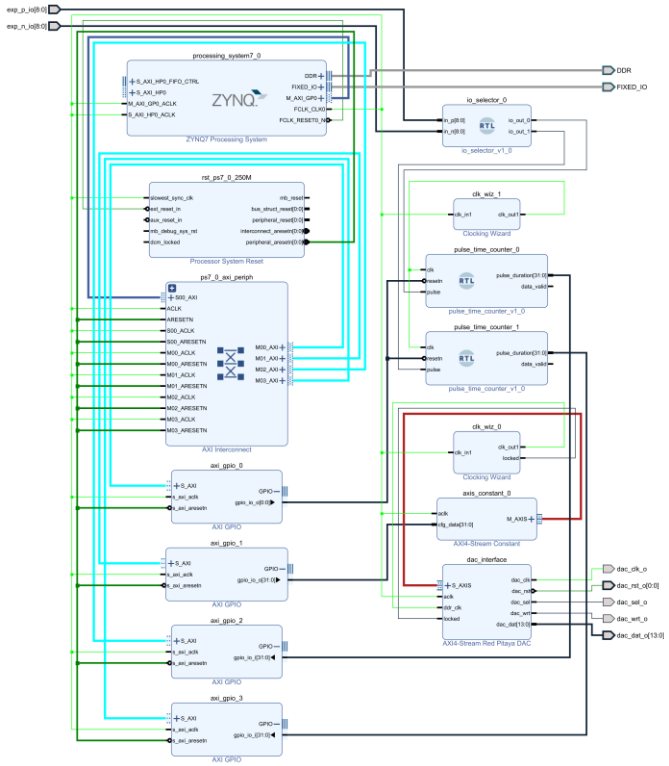


Fig. 5. FPGA Programmable Logic (PL) design schematic showing the implementation of dual-channel pulse timing, AXI interfaces, and DDR DAC control for adaptive thresholding

The outputs of the threshold comparators are directed to specialized Pulse-time Counters implemented within the FPGA fabric. These counters measure the time the input signal is above each threshold, effectively quantizing the Time-over-Threshold (ToT) for the lower and upper thresholds. Having two thresholds in the DToT approach gives a more complete characterization of the input signal than single threshold methods.

Following the Pulse-time Counters, the system incorporates I/O interfaces to manage data flow between the counters and the FPGA's internal memory. These interfaces handle tasks like data formatting, buffering, and synchronization to ensure data is transferred reliably in the FPGA's high-speed digital environment. The processed ToT measurements are then stored in the FPGA's memory to create a repository of timing data for later analysis.

FPGA Programmable Logic (PL) is shown in Fig. 5. The *io_selector* block handles the input stage, the interface for digital inputs. This block manages multiple digital I/Os from the board, the differential input arrays *exp_p_io* and *exp_n_io* for positive and negative signals, respectively. In this application, only two single-ended inputs are used, input0 and input1. The *io_selector* filters these two inputs from the larger array and directs them to separate pulse-time counters for further processing.

Two *pulse_time_counter* blocks are the heart of the timing measurement system. These counters measure pulse widths with high precision using a 400 MHz clock generated by *clk_wiz_1*. Two separate counters allow us to measure two

input channels simultaneously for comparison or redundancy in timing measurements.

AXI GPIO (General Purpose Input/Output) blocks are used for data transfer between the FPGA fabric and the ARM CPU. Four blocks (*axi_gpio_0* to *axi_gpio_3*) are implemented for a robust bi-directional data transfer. These GPIO blocks are critical to the system so the CPU can read the measured pulse times from the counters and send control signals and configuration data back to the FPGA logic.

A key feature of this design is dynamic threshold adjustment, which is important for adaptive signal processing in changing conditions. This is done using a two-channel DAC connected directly to the FPGA. The CPU adjusts the lower and upper threshold comparator voltages by sending the desired levels to a custom *dac_interface* block via the GPIO interface. This block formats and manages the data stream to the DAC to adjust the threshold precisely and in time. Such adaptability enhances the system's performance across diverse nuclear spectroscopy scenarios, particularly in environments with fluctuating background radiation or varying signal intensities.

The DAC interface is configured to operate in Double Data Rate (DDR) mode, a high-efficiency data transmission technique that maximizes the data transfer rate. In this configuration, the DAC voltage for channel one is applied on the rising edge of the clock signal, while channel two is updated on the falling edge. This approach effectively doubles the data rate without increasing the base clock frequency, allowing for rapid and synchronized updates of both threshold levels.

The design has an advanced clock management solution to facilitate the DAC's DDR operation. While the system's base clock operates at 125 MHz, the DDR interface needs a clock signal at twice this frequency. A clock management module (*clk_wiz_0*) generates the required 250 MHz signal, ensuring proper timing for the DDR DAC interface. This precisely controlled higher-frequency clock enables accurate and timely updates of threshold voltages, which is critical for the overall timing accuracy and measurement precision in nuclear spectroscopy applications.

III. Results

I implemented single and double ToT methods in the FPGA and used a detector emulator (CAEN DT4800) to test the linearity of the relationship between input pulse amplitude and time width.

A. Single-Threshold ToT Results

Fig. 6 shows the input amplitude spectrum (solid line) and the estimated amplitude spectrum (dashed line) from single-threshold ToT measurements. Two photo-peaks at 511 keV and 1275 keV from ^{22}Na decay are visible. The close match between the input and estimated spectra at these photo-peaks proves that the FPGA design works well for reconstructing the original signal amplitude. This demonstrates that our approach can accurately estimate signal amplitudes from ToT measurements, even with a single-threshold configuration.

B. Double-Threshold ToT Results

Fig. 7 presents a comparison between the input amplitude spectrum (represented by a solid line) and the estimated amplitude spectrum (shown as a dashed line) obtained using double-threshold time-over-threshold (DToT) measurements. The graph is normalized to amplitude in millivolts and shows two photo-peaks at 511 keV and 1275 keV. This comparison indicates that the DToT works well for reconstructing the original signal amplitude. The close alignment between the input and estimated spectra, particularly at these key photo-peaks, validates the precision of the FPGA-based approach.

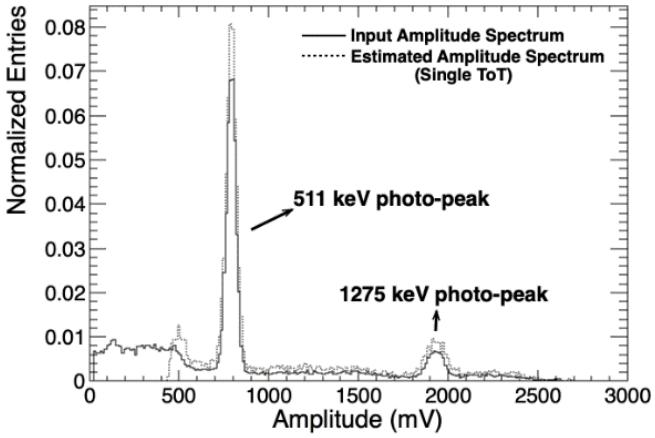


Fig. 6. Comparison of input amplitude spectrum (solid line) with estimated amplitude spectrum (dashed line) using **single-threshold time-over-threshold** measurements.

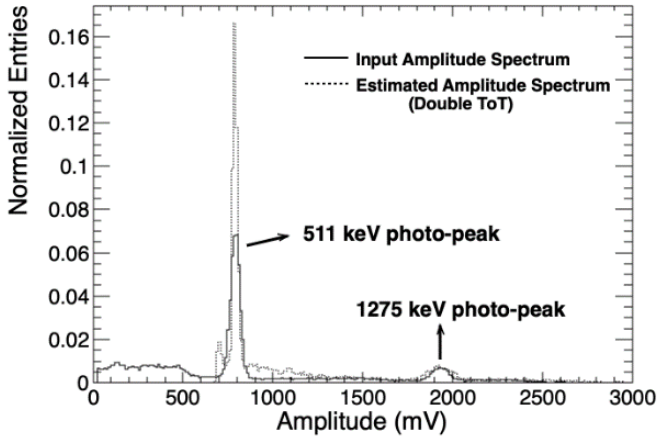


Fig. 7. Comparison of input amplitude spectrum (solid line) with estimated amplitude spectrum (dashed line) using **DToT** measurements.

The DToT has better resolution and accuracy than single threshold methods, especially at the 511 keV peak. This improved spectral reconstruction benefits the DToT measurement system and shows its potential for high-precision particle detection and energy discrimination in many applications.

Table I presents a comparative analysis of photo-peak locations for the input spectrum, single ToT estimates, and double ToT estimates at 511 and 1275 keV. The input spectrum peaks at 789.78 ± 28.95 mV for 511 keV, while the single and double ToT estimates are at 789.83 ± 31.50 mV and 789.72 ± 14.34 mV, respectively. Similarly, there is a peak at 1929.72 ±

65.98 mV for 1275 keV, while the single and double ToT estimates are at 1927.95 ± 73.30 mV and 1931.44 ± 73.76 mV, respectively. The DToT has better precision at 511 keV with a much lower standard deviation. To further evaluate the performance, I look at the σ/μ ratio, which is the indicator for detector resolution. For the 511 keV peak, these ratios are

TABLE I
PHOTO-PEAK LOCATIONS OF INPUT SPECTRUM, SINGLE AND DOUBLE TOT ESTIMATES

Photo-peak location in mV		
Spectrum Type	511 keV (μ±σ)	1275 keV (μ±σ)
Input Spectrum	789.78±28.95	1929.72±65.98
Single ToT Estimate	789.83±31.50	1927.95±73.30
Double ToT Estimate	789.72±14.34	1931.44±73.76

3.67%, 3.99%, and 1.82% for the input, single ToT, and double ToT methods, respectively. At 1275 keV, the ratios are 3.42%, 3.80%, and 3.82%. These results indicate that the DToT method offers a marked improvement in energy resolution at lower energies while maintaining comparable performance at higher energies. This enhancement in precision, particularly at lower energies, underscores the potential advantages of the DToT technique in applications requiring high-resolution spectroscopy.

C. Limitations and Future Directions

The cutoff values in the signal amplitude estimates are defined by the lower threshold levels at 50 mV, which is the lowest possible threshold due to the noise in the system. At lower energies near the Compton edge, the signal amplitude estimates produce an artificial photo-peak, suggesting a careful analysis near the measurements at lower threshold values.

The enhanced resolution and accuracy of the DToT method, particularly at lower energies, make it highly suitable for applications requiring precise energy discrimination in nuclear spectroscopy. The ability to maintain comparable performance at higher energies further underscores the versatility of the DToT technique.

While the DToT method shows promising results, there are limitations to consider. The artificial photo-peak observed near the lower threshold suggests the need for careful analysis in certain energy ranges. Future studies could explore optimizing the system for specific experimental setups, such as scintillation gamma cameras or positron emission tomography, to fully realize the potential of the DToT method.

IV. CONCLUSIONS

The FPGA-based system I designed implements single and double ToT measurement techniques. Fig. 2 and Fig. 3 display the input amplitude spectra and the corresponding estimated amplitude spectra for single and double ToT measurements. The comparison between these spectra shows that the DToT method yields better energy resolution compared to the single ToT approach.

The architecture of this FPGA-based system combines an ARM processing system with customized FPGA logic. Advanced eXtensible Interface (AXI) protocols allow the integration of standard IP cores and custom logic, making the system more modular. The system includes dual pulse-time counters, a DDR DAC interface allowing dynamic threshold adjustment for adaptive signal processing, FPGA-based parallel processing circuits to minimize latency, and an integrated ARM CPU for complex algorithm implementation and system control.

Having dual pulse-time counters with dynamic threshold adjustment via the DDR DAC interface provides a DToT platform for applications requiring precise timing measurements and adaptive signal processing. This could be particularly valuable in nuclear physics and related fields, where accurate timing and amplitude measurements of signal pulses are critical.

This study presents an FPGA-based signal processing system that combines adaptive thresholding with high-precision timing measurements, allowing amplitude estimations after linearity correction. The system's architecture allows for the customization of data processing algorithms, enabling its application in particle physics experiments, medical imaging systems, and industrial sensors. Future work could explore its performance in specific experimental setups, such as scintillation gamma cameras or positron emission tomography, potentially leading to optimized configurations for each application domain.

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